Improved Stability With Atomic-Layer-Deposited Encapsulation on Atomic-Layer In_2O_3 Transistors by Reliability Characterization

Adam Charnas, Mengwei Si, *Member, IEEE*, Zehao Lin, and Peide D. Ye, *Fellow, IEEE*

***Abstract*—Ultrathin In_2O_3 and other recently explored low-thermal-budget ultrathin oxide semiconductors have shown great promise for back-end-of-line (BEOL)-compatible logic layers and monolithic 3-D (M3-D) integration. However, the long-term stability and reliability of these defect-rich atomically thin channels have not been intensively explored yet. Here, we present a study of the long-term reliability of transistors with 1.2-nm-thick atomic-layer-deposited (ALD)-grown In_2O_3 channels by room-temperature positive bias instability (PBI) and negative bias instability (NBI) experiments. The observed behavior can be largely explained by a trap neutrality level (TNL) model. A route to reduce the parameter drift has been developed using encapsulation in sequence with V_T engineering by an O_2 plasma treatment. After treatment, the magnitude of long-term V_T shift is reduced for both positive and negative gate bias stresses, and for negative bias stress, other transistor parameters are stabilized as well. In all cases, the subthreshold swing (SS) does not change over time, suggesting that stress-induced interface defects form far below the conduction band, if at all.**

***Index Terms*—Atomic-layer deposition (ALD), back-end-of-line (BEOL) compatible, bias instability (BI), encapsulation, indium oxide, oxide semiconductor, thin-film transistor.**

I. Introduction

RECENTLY, transistors with channels made of ultrathin layers of oxide semiconductors with nanometer-scale thickness have been investigated by several groups, showing impressive device performance on a low thermal budget with wafer-scale uniformity [1], [2], [3], [4], [5], [7], [8], [9]. Putting indium oxide's degenerate carrier concentration in check by quantum confinement in the ultrathin limit [9] enables effective gate control with I_{ON}/I_{OFF} ratios better than 10^8 achievable with record high on current, and the symmetry of the s-orbital-dominated conduction band gives disorder-resistant mobility [10] up to $\sim$113 $cm^2/V \cdot s$ for devices annealed at 350 °C [11], [12]. These results are exciting developments toward high-performance back-end-of-line (BEOL) logic and monolithic 3-D (M3-D) integration.

Devices with atomic-layer thin oxide channel thickness have not been studied until recently. Among the avenues of investigation of immediate importance is the question of long-term stability and reliability, which is critical for real-world applications, where devices may be expected to have a ten-year lifetime with minimal parameter drift. Since oxide semiconductor channels at the nanometer scale are largely unstudied and the interface chemistry—which plays a key role in device stability—is markedly different from 2-D van der Waals materials, the basic characterization studies are needed. Furthermore, routes must be identified to potentially improve the stability, and since In_2O_3 is well-suited for BEOL and M3-D applications, the thermal budget should remain within tight constraints. In this article, the reliability of ultrathin In_2O_3 transistors is investigated by room-temperature negative bias instability (NBI) and positive bias instability (PBI) experiments at a variety of biases. It is found that significant improvements to the long-term bias instability (BI) parameter drifts can be obtained by capping the devices with a thin atomic-layer-deposited (ALD) HfO_2 encapsulation layer. HfO_2 was chosen because the interface between In_2O_3 and HfO_2 has been studied in previous works [13], appears reasonably clean, and can be readily improved by O_2 plasma treatment [14].

Bias temperature instabilities are gradual shifts in the operating characteristics of transistors driven by applied voltage, temperature, or a combination thereof. In modern Si CMOS, they have become a major reliability concern and significant research efforts have been directed toward identifying the root causes and reducing the resulting parameter drifts [15], [16]. Significant debate remains as to the physical origin of these phenomena [17], [18], [19], and however,

Manuscript received 27 July 2022; accepted 9 August 2022. Date of publication 24 August 2022; date of current version 22 September 2022. This work was supported in part by the Semiconductor Research Corporation (SRC) the nanoelectronic COmputing REsearch (nCore) the Innovative Materials and Processes for Accelerated Compute Technologies (IMPACT) Center and in part by the SRC/Defense Advanced Research Projects Agency (DARPA) Joint University Microelectronics Program (JUMP) Applications and Systems Drive Center for Energy-Efficient Integrated Nano Technologies (ASCENT) Center. The review of this article was arranged by Editor J.-S. Park. *(Corresponding author: Peide D. Ye.)*

The authors are with the School of Electrical and Computer Engineering and the Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3198926.

Digital Object Identifier 10.1109/TED.2022.3198926

0018-9383 © 2022 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: Purdue University. Downloaded on October 13,2022 at 17:17:37 UTC from IEEE Xplore. Restrictions apply.

it is understood that there are multiple mechanisms behind the shifts. The culprit is thought to be a combination of carrier trapping at the semiconductor–dielectric interface and in the gate dielectric (both in existing traps and stress-induced traps) [18].

II. Experiment

The device structure is shown in Fig. 1(a) with an outline of the fabrication steps given in Fig. 1(b). The device fabrication process is similar to those in [11], [12], [13], and [14]. A 4-in silicon wafer capped with 90-nm SiO_2 is solvent cleaned with a series of ultrasonic baths in toluene, acetone, and isopropanol for 5 min each and dried with N_2. A bilayer photoresist structure is spin coated using SF9 [polydimethylglutarimide (PMGI)] followed by AZ1518 to yield an undercut profile after development for clean lift-off. The buried gate regions are exposed by photolithography and developed by soaking in MF-26A; 40-nm Ni for the gate contacts is deposited by electron beam evaporation followed by lift-off in Remover PG at 80 °C and further solvent cleaning to minimize residues. Next, the gate dielectric (5-nm HfO_2) and channel (1.2-nm In_2O_3) materials are grown by ALD at 200 °C and 225 °C, respectively. The metal-organic precursors used are $[(CH_3)_2N]_4Hf$ (TDMAHf) and $(CH_3)_3In$ (TMIn) with H_2O as the oxygen source in both cases. After ALD, the samples are spin coated with AZ1518 photoresist and the In_2O_3 channel regions are defined by photolithography and isolated by wet etching in concentrated HCl. Finally, ZEP 520A electron beam resist is spin coated and the source and drain contact regions are defined by electron beam lithography and developed in ZED-N50; 60-nm Ni for the contacts was deposited by electron beam evaporation followed by lift-off in ZDMAC at 50 °C. Some samples receive additional encapsulation by 1.6-nm HfO_2 grown by ALD at 200 °C and further treatment by O_2 plasma [14], which is found to reduce bias instabilities. The encapsulation process is also effectively an extended anneal at 200 °C, and however, this is lower than the temperature that In_2O_3 is grown at and hence likely does not contribute much to device performance [12].

BI data were collected using a semiconductor parameter analyzer for a variety of devices with and without treatment at room temperature. Devices were placed in an enclosed probe station under nitrogen flow at atmospheric pressure during measurement. A measurement–stress–measurement scheme was used with a short delay between stress and measure segments of 1 ms and moderate integration time to limit recovery, similar to [15]. During stress, the gate was biased at a fixed voltage, while the source, drain, and substrate were grounded. Bias stress was interrupted on a logarithmic time scale up to 3000 s to collect transfer characteristics with a low drain bias of 50 mV. The inherent delay of using a parameter analyzer rather than a specialized setup with μs delay [22], and collecting full transfer characteristics rather than estimating ΔV_T from a single point or few points, means that the data presented here are blind to some short-timescale dynamics. Thus, the absolute rate of V_T shift should not be read into too

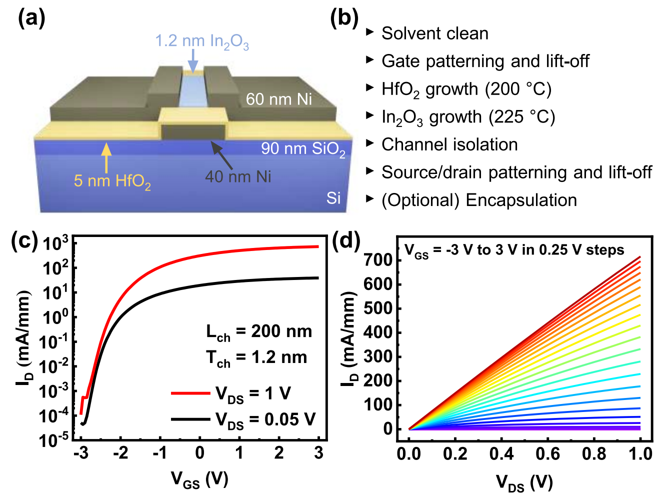

Fig. 1. (a) Device structure and (b) fabrication process outline. Example (c) transfer and (d) output characteristics of a device with $L_{ch} = 200$ nm after encapsulation and O_2 plasma treatment, demonstrating excellent dc performance.

much. However, the key point is that the long-term reliability of these devices has been explored and HfO_2 capping improves that reliability. The reported values of V_T were extracted using linear extrapolation of the transfer curves from the point of maximum g_m, except where noted. Since this technique can be sensitive to mobility degradation, V_T was also extracted with the transconductance derivative, constant current, and drain conductance ratio methods. In general, the trends observed are the same. As is typical, the devices recover from stress quickly following a decaying exponential trend.

III. Results and Discussion

Devices over a wide range of channel lengths from $L_{ch} = 1$ μm to 60 nm have been studied under gate bias stresses of ± 1, ± 2, and ± 3 V. This roughly corresponds to $|E_{ox}| = 2$, 4, and 6 MV/cm, respectively, with some margin of error due to the sub-nanometer thin nickel oxide layers formed on the metal contacts. Higher biases will push the HfO_2 gate dielectric layer to break down. Transfer (I_D–V_{GS}) and output (I_D–V_{DS}) characteristics for a sample device with $L_{ch} = 200$ nm are shown in Fig. 1(c) and (d), respectively. The low subthreshold swing (SS), ohmic contacts, and high I_{ON} can be seen.

Detailed statistical characterizations of key dc performance metrics of the devices are shown in Fig. 2 as functions of channel length. Error bars represent one standard deviation from the average of at least five devices. Data for three cases are shown: 1) initial measurements of the devices after fabrication; 2) measurements after encapsulating the devices in 1.6-nm ALD HfO_2 grown at 200 °C; and 3) measurements after a subsequent room-temperature O_2 plasma treatment [14]. The HfO_2 capping layer initially shifts V_T negatively by several volts as shown in Fig. 2(b), which could be due to a large amount of fixed positive charges in low-temperature grown ALD films. This effect is widely observed in 2-D van der Waals materials research and is sometimes called the dielectric

Authorized licensed use limited to: Purdue University. Downloaded on October 13,2022 at 17:17:37 UTC from IEEE Xplore. Restrictions apply.

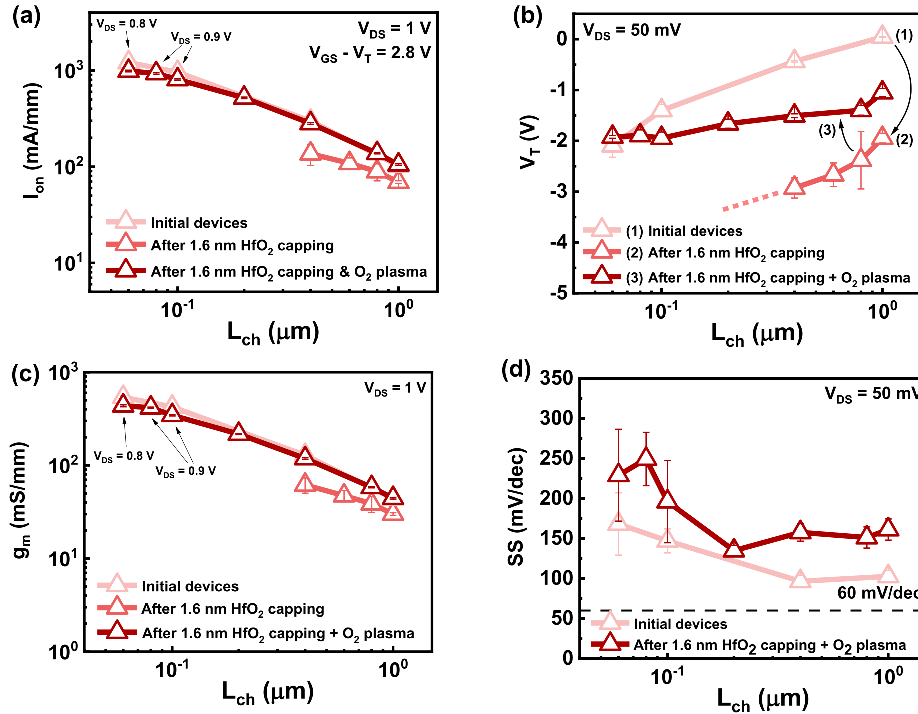

Fig. 2. DC characterization of the ultrathin In_2O_3 TFTs studied, demonstrating the effects of 1.6-nm ALD HfO_2 capping and subsequent O_2 plasma treatment. (a) ON current at $V_{GS} - V_T = 2.8$ V with $V_{DS} = 1$ V except where noted. (b) Threshold voltage extracted by linear extrapolation. Arrows indicate the order of treatments applied to the devices. For the second case with HfO_2 encapsulation but without O_2 plasma treatment, V_T becomes very negative and cannot be measured at short-channel lengths. (c) Transconductance. (d) SS. Since V_T is so negative for the encapsulated devices without plasma treatment, SS cannot be meaningfully measured. Error bars represent one standard deviation from the average of at least five devices.

doping effect [20]. The rate of short-channel V_T roll-off is also increased, perhaps due to the introduction of more defects in the In_2O_3 by chemical interaction with the encapsulation layer, such as the scavenging of oxygen by Hf [21], which could also increase the effective n-type doping of the channel, resulting in the negative V_T shift. This undesirable V_T shift is the reason for the subsequent O_2 plasma treatment since a previous study has revealed that it can shift V_T positively—likely due to the elimination of oxygen vacancies in In_2O_3 and reduction of defects at the In_2O_3/HfO_2 interface [14]. The plasma treatment used here is the same detailed in [14]: the devices are exposed to O_2 plasma (1.25 torr) in a barrel asher at room temperature with 100 W of RF power. Without the O_2 plasma treatment, V_T is too negative to access the subthreshold regime at most channel lengths studied, as shown in Fig. 2(b). This is why SS data are not given for the HfO_2 encapsulated devices without plasma treatment in Fig. 2(d). With this combined treatment, the excellent overall dc performance of the devices is largely maintained in terms of I_{ON}, I_{ON}/I_{OFF} ratio, and mobility with a small V_T shift and slightly elevated SS, and the long-term bias stress stability is improved without adding significant complexity to the device fabrication process.

By thickness control [13], annealing [11], [12], O_2 plasma treatment [14], and dielectric encapsulation, ultrathin In_2O_3 devices have been demonstrated with I_{ON} well above 2 A/mm, the I_{ON}/I_{OFF} ratio around 10^{10}, field-effect mobility up to 113 $cm^2/V \cdot s$, transconductance approaching 1 S/mm, and SS near the room-temperature thermionic limit of 60 mV/dec.

TABLE I

LOW-BIAS PARAMETER DRIFTS FOR UNTREATED DEVICES AFTER 3000 S

Bias	ΔV_T (mV)	ΔI_{on} (%)[a]	$\Delta \mu_{FE}$[b] ($cm^2/V \cdot s$)	Δg_m (mS/mm)	ΔSS (mV/dec)
+1 V	-27.5	0.05	-0.04	-0.002	0.07
-1 V	-58.4	0.52	0.05	0.005	-5.85

Cumulative measured parameter drifts of un-treated devices after 3000 s of moderate positive or negative gate bias stress at room temperature. The devices are very stable under these operating conditions, even without treatment.

[a] I_{on} is calculated at a constant gate overdrive voltage ($V_{GS} - V_T$) of 3 V.

[b] C_{ox} measurements used to extract μ_{FE} can be found in Refs. [13-14]. A value of 1.6 $\mu C/cm^2$ is used.

Here, we choose some of these novel devices and investigate their stability and reliability through systematic NBI and PBI studies at room temperature.

NBI data at a high stress bias are summarized in Fig. 3 to show worst case accelerated degradation. In typical mature logic applications, a significantly lower supply voltage (V_{DD}) would be applied, resulting in much slower degradation. Representative measured results of this type with $V_{GS} = 1$ V are summarized in Table I showing minimal parameter shifts for both NBI and PBI. The trajectories of the high-bias NBI transfer curves of example treated and untreated devices with $L_{ch} = 1$ μm are plotted in Fig. 3(a) for direct comparison. The curves in both cases gradually shift left over time as a result of net accumulation of positive charge in the vicinity of

Authorized licensed use limited to: Purdue University. Downloaded on October 13,2022 at 17:17:37 UTC from IEEE Xplore. Restrictions apply.

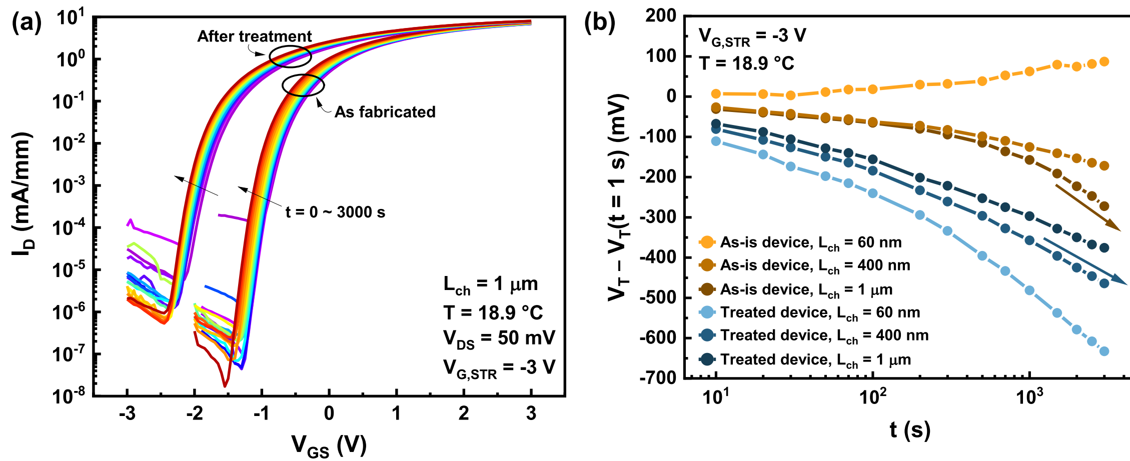

Fig. 3. NBI characterization of devices before and after treatment at a high gate stress bias of −3 V. (a) Transfer characteristics of sample devices before (right) and after (left) treatment over the course of 3000 s under negative gate bias stress. (b) V_T shift referenced to V_T measured after 1 s of stress. For the 60-nm as-is device, ΔV_T is extracted by the constant current method due to the large negative V_T. V_T quickly shifts by about 100 mV during the initial seconds of stress due to fast states, and then, the long-term rates of shift are roughly similar. This may be improved by a detailed future study of passivation and is less important for n-type devices than the PBI.

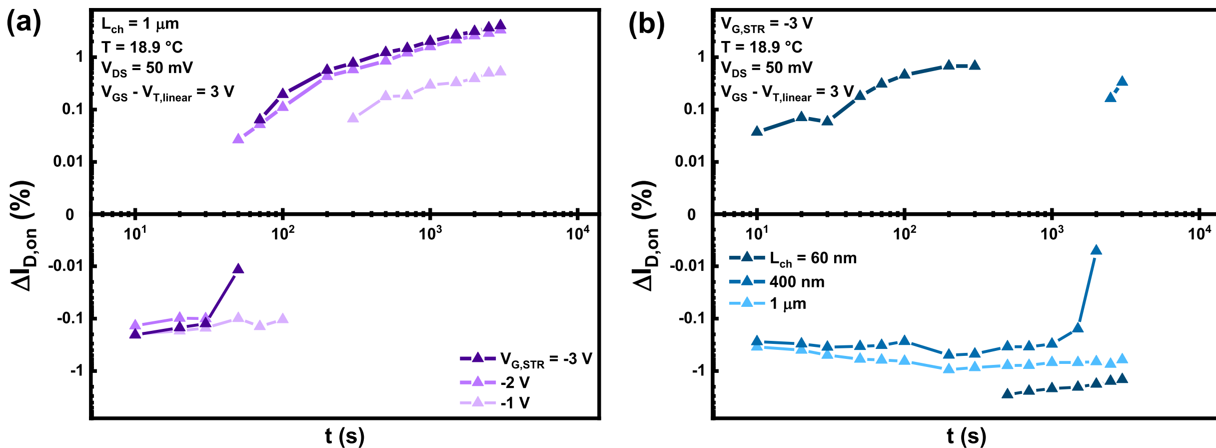

Fig. 4. NBI on current shift for (a) untreated devices as a function of time and stress voltage and (b) devices after 1.6-nm HfO_2 capping and O_2 plasma treatment as a function of time and channel length at the highest stress bias tested. Before treatment, the ON current slowly increases over time as a function of the applied bias stress, ultimately shifting by up to several percents over 3000 s. A clear linear trend develops by the end of measurement. After treatment, the drain current appears more stable, tending to mostly stay flat with less than a 1% net shift despite the large stress voltage applied.

the dielectric–semiconductor interface. Fig. 3(b) shows the V_T shifts of the same devices over time in addition to two other treated and untreated devices with shorter channel lengths. A point of interest is that the magnitude of NBI V_T shift is slightly elevated for the treated devices due mainly to fast states that rapidly charge in the early seconds of stress time. Fortunately, the V_T shift is still relatively small considering the strength of the applied electric field, and NBI behavior is not as important as PBI for these devices that are proposed to be used mainly for switching logic. On a typical chip, the gate would swing between positive V_{DD} and ground. The observed differences in behavior between different channel length devices are attributed to different electrostatics across the length of the channel. Trapping effects depend on both local temperature and electric field, which will be different in the center of the channel versus nearby and under the source and drain contacts. As the channel length scales down, the proportion of the device in proximity to the source and drain contacts increases. Minor changes in ON-current over time are summarized in Fig. 4.

Fig. 5 shows the trajectories of devices subject to a large positive bias stress of +3 V to accelerate their degradation. In Fig. 5(a), the differences between treated and untreated devices are more immediately apparent than they were for the NBI case. This can also be clearly seen in the V_T shifts extracted in Fig. 5(b). The long-term rate of V_T shift is greatly reduced after treatment and there are clear directional differences, suggesting rebalancing of the rates of the different degradation mechanisms. Fig. 6 summarizes the change in ON current for the same set of devices. In contrast to the

Authorized licensed use limited to: Purdue University. Downloaded on October 13,2022 at 17:17:37 UTC from IEEE Xplore. Restrictions apply.

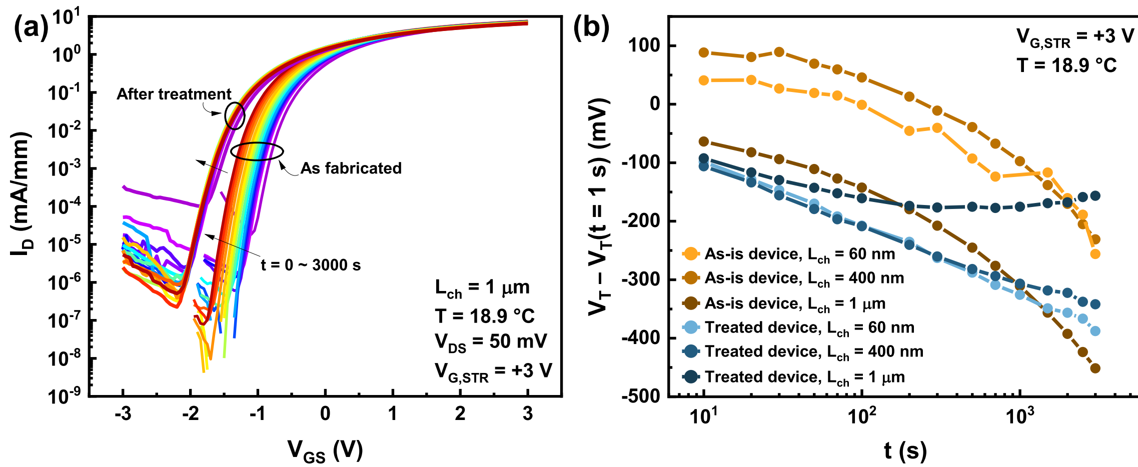

Fig. 5. PBI characterization of devices before and after treatment at a high gate stress bias of +3 V. (a) Transfer characteristics of sample devices before (right) and after (left) treatment over the course of 3000 s under positive gate bias stress. (b) VT shift referenced to VT measured after 1 s of stress. The long-term VT shift slope of the treated devices is significantly reduced, and a reversal of direction is observed for the long-channel device.

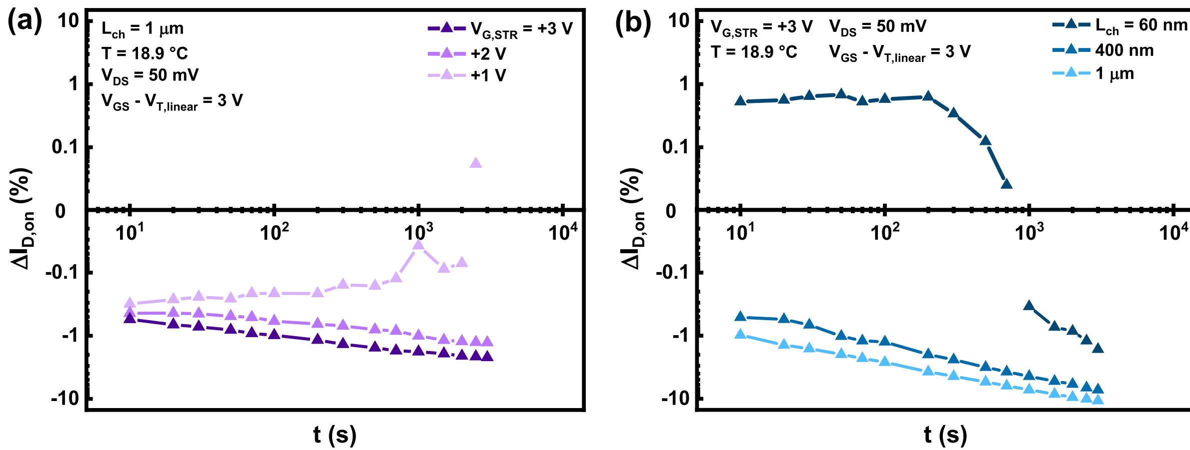

Fig. 6. PBI on current shift for (a) untreated devices as a function of time and stress voltage and (b) devices after 1.6-nm HfO_2 capping and O_2 plasma treatment as a function of time and channel length at the highest stress bias. Without treatment, the ON current is reasonably stable, tending to gradually decrease over time as a function of the applied bias stress with the exception of +1-V stress, ultimately shifting by a couple percent over 3000 s. The degradation follows a clear linear trend. After treatment, the drain current appears a little less stable, drifting at a faster pace.

negative bias stress results, ON-current degradation does not improve under positive bias stress after HfO_2 capping and O_2 plasma treatment. However, the magnitude of shift is less for shorter channel lengths and is greatly reduced at a lower, more realistic, gate bias (see Table I).

Fig. 7 shows the time evolution of the SS of devices subject to the highest gate bias stresses measured with $L_{ch} = 1$ μm. In all cases, the SS does not change appreciably over time (including for lower stress voltages). If new interface traps form as a result of stress, this suggests that energetically, they are forming well away from the conduction band, far from the region that our electrical measurements probe. It is worth noting that the HfO_2 capping treatment does appear to result in a slight increase in the SS. Due to their ultrathin channels, the devices studied here are essentially entirely surface. It becomes hard to distinguish the surface and interface from the bulk channel once the channel is as thin as 1.2 nm at the atomic layer level.

Fig. 8 gives a simple model to qualitatively explain the observed V_T shifts under stress. The trap neutrality level (TNL) model is used to explain the behavior at semiconductor/insulator interfaces and is effectively similar but fundamentally different to the charge neutrality level (CNL) concept employed for semiconductor/metal interfaces [9], [23], [24]. This level represents the branch point of the interface states, above which states are called donor trap states and electrically positive if empty and below which states are called acceptor trap states and electrically neutral if filled. A U-shaped effective interface trap density profile is widely observed in semiconductor/oxide interface such as in the Si/SiO_2 interface. For In_2O_3, the uniqueness is its special band alignment whose TNL or CNL is located deep above the conduction band edge

Authorized licensed use limited to: Purdue University. Downloaded on October 13,2022 at 17:17:37 UTC from IEEE Xplore. Restrictions apply.

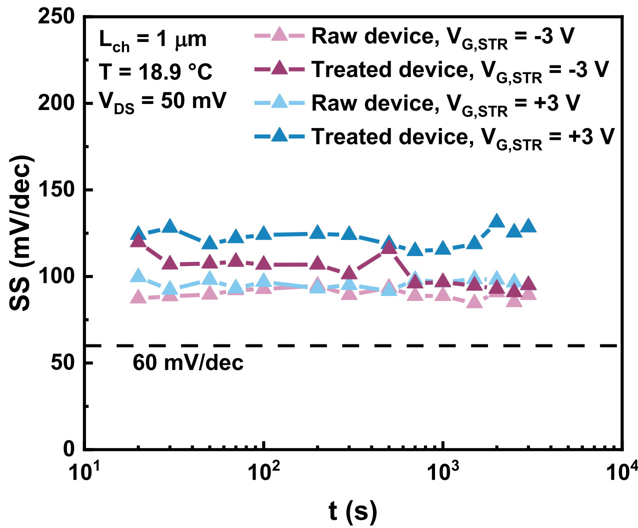

Fig. 7. In all cases, the SS does not change appreciably over the duration of stress measurement. This shows that new interface traps, if any, are not generated in the vicinity of E_F.

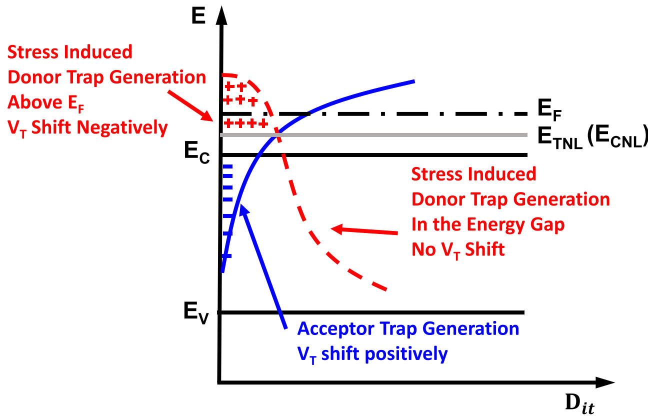

Fig. 8. Model for the observed V_T shifts with the simple D_{it} profile at the HfO_2/In_2O_3 interface with acceptor/donor traps. The Fermi level is above the TNL in the depletion-mode operation. It explains why V_T shifts left for both NBI and PBI cases. Because of In_2O_3's large valence DOS or its unique band alignment, the TNL is located above the conduction band edge or deeply inside the conduction band.

due to its large density of valence band states [26], [27]. The as-grown ALD In_2O_3 has high electron charge density and negative V_T for its devices so that E_F is far above E_{TNL} in the normal operation. Regardless of the polarity of stress voltage applied (PBI or NBI), there will be a distribution of donor-like interface states above E_{TNL} and generate more donor-like interface trap states that are empty and positively charged when E_F moves down at the subthreshold region, leading to the general V_T shifting to the left. Under the PBI test as shown in Fig. 5, more positively charged donor trap states are generated so that V_T shifts to left or more negative in the experiments. Dielectric capping passivates some donor-like traps so that V_T shift is less than uncapped one and PBI is improved. Under the NBI test, E_F moves down through E_{TNL} and even inside bandgap. The stress could generate much more donor traps and even some acceptor traps inside bandgap. Acceptor-like trap density inside bandgap is small, as shown in Fig. 8, and once E_F moves back to the subthreshold region or E_F above or near E_{TNL}, the dominated trap type, which is electrically active, is still donor-like traps and V_T still shifts to left or more negatively. After passivation or dielectric capping, all donor/acceptor-like trap density might be reduced. However, the donor-like trap density under E_{TNL} is much more than that above E_{TNL}, as shown in Fig. 8. This leads to the effect of dielectric passivation that is less obvious in experiments, as presented in Fig. 3.

There must be further room to improve the reliability behavior of these devices with deeper understanding of the reliability physics in this new channel material. The work presented here is the first attempt to address reliability issues on these novel devices. In particular, the short-term V_T shift is still higher than the desirable one. A more mature process with fewer preexisting traps in the oxide may lead to improvements, as discussed in [15] and [16]. A more optimized O_2 plasma treatment with other surface chemistry or an annealing step may also lead to further reductions in parameter drift.

IV. Conclusion

Initial investigation into the bias stress instability behavior of ultrathin In_2O_3 TFTs has shown that they are quite stable in gentle conditions, i.e., at room temperature under low biases. A TNL model is able to qualitatively explain the direction of V_T shifts observed. Treating the devices by HfO_2 encapsulation has been demonstrated to reduce the V_T shift magnitude and rate under long-term stresses, and furthermore, it is demonstrated that the parameter improvements from O_2 plasma treatment are robust and do not disappear over time. There is still more room for improvement by reducing the short-term V_T shifts, which requires more understanding of the origin of the traps in this new material system and the development of more mature processing.

References

[1] M. Si *et al.*, "Indium–tin-oxide transistors with one nanometer thick channel and ferroelectric gating," *ACS Nano*, vol. 14, no. 9, pp. 11542–11547, Aug. 2020.

[2] S. Li *et al.*, "Nanometre-thin indium tin oxide for advanced high-performance electronics," *Nature Mater.*, vol. 18, no. 10, pp. 1091–1097, Aug. 2019.

[3] S. Li *et al.*, "BEOL compatible 15-nm channel length ultrathin indium-tin-oxide transistors with I_{on} = 970 μA/μm and on/off ratio near 10^{11} at V_{ds} = 0.5 V," in *IEDM Tech. Dig.*, Dec. 2019, pp. 3.5.1–3.5.4.

[4] W. Chakraborty, B. Grisafe, H. Ye, I. Lightcap, K. Ni, and S. Datta, "BEOL compatible dual-gate ultra thin-body W-doped indium-oxide transistor with I_{on} = 370 μA/μm. SS = 73 mV/dec and I_{on}/I_{off} ratio > 4×10^9," in *Proc. Symp. VLSI Technol.*, Jun. 2020, pp. 1–2.

[5] S. Samanta, K. Han, C. Sun, C. Wang, A. V.-Y. Thean, and X. Gong, "Amorphous IGZO TFTs featuring extremely-scaled channel thickness and 38 nm channel length: Achieving record high Gm,max of 125 μS/μm at V_{DS} of 1 V and I_{ON} of 350 μA/μm," in *Proc. Symp. VLSI Technol.*, Jun. 2020, pp. 1–2.

[6] J. Lee *et al.*, "High mobility ultra-thin crystalline indium oxide thin film transistor using atomic layer deposition," *Appl. Phys. Lett.*, vol. 113, no. 11, Sep. 2018, Art. no. 112102.

[7] T. J. Yen, A. Chin, and V. Gritsenko, "High-performance top-gate thin-film transistor with an ultra-thin channel layer," *Nanomaterials*, vol. 10, no. 11, p. 2145, Oct. 2020.

[8] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 45, pp. 4303–4308, May 2006.

Authorized licensed use limited to: Purdue University. Downloaded on October 13,2022 at 17:17:37 UTC from IEEE Xplore. Restrictions apply.

[9] M. Si *et al.*, “Why In_2O_3 can make 0.7 nm atomic layer thin transistors,” *Nano Lett.*, vol. 21, no. 1, pp. 500–506, Jan. 2021.

[10] T. Kamiya, K. Nomura, and H. Hosono, “Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping,” *J. Display Technol.*, vol. 5, no. 12, pp. 468–483, Dec. 2009.

[11] M. Si, A. Charnas, Z. Lin, and P. D. Ye, “Enhancement-mode atomic-layer-deposited In_2O_3 transistors with maximum drain current of 2.2 A/mm at drain voltage of 0.7 V by low-temperature annealing and stability in hydrogen environment,” *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1075–1080, Mar. 2021.

[12] M. Si *et al.*, *Proc. Symp. VLSI Technol.*, Jun. 2021, p. T2-4.

[13] M. Si, Z. Lin, A. Charnas, and P. D. Ye, “Scaled atomic-layer-deposited indium oxide nanometer transistors with maximum drain current exceeding 2 A/mm at drain voltage of 0.7 V,” *IEEE Electron Device Lett.*, vol. 42, no. 2, pp. 184–187, Feb. 2021.

[14] A. Charnas, M. Si, Z. Lin, and P. D. Ye, “Enhancement-mode atomic-layer thin In_2O_3 transistors with maximum current exceeding 2 A/mm at drain voltage of 0.7 V enabled by oxygen plasma treatment,” *Appl. Phys. Lett.*, vol. 118, no. 5, Feb. 2021, Art. no. 052107.

[15] S. Pae *et al.*, “BTI reliability of 45 nm high-K + metal-gate process technology,” in *Proc. IEEE Int. Rel. Phys. Symp.*, May 2008, pp. 352–357.

[16] K. T. Lee *et al.*, “Technology scaling on high-K & metal-gate FinFET BTI reliability,” *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2013, pp. 2D.1.1–2D.1.4.

[17] J. H. Stathis, S. Mahapatra, and T. Grasser, “Controversial issues in negative bias temperature instability,” *Microelectron. Rel.*, vol. 81, pp. 244–251, Feb. 2018.

[18] S. Mahapatra and N. Parihar, “A review of NBTI mechanisms and models,” *Microelectron. Rel.*, vol. 81, pp. 127–135, Feb. 2018.

[19] D. P. Ioannou, “HKMG CMOS technology qualification: The PBTI reliability challenge,” *Microelectron. Rel.*, vol. 54, no. 8, pp. 1489–1499, Aug. 2014.

[20] G. Qiu *et al.*, “Quantum Hall effect of Weyl fermions in n-type semiconducting tellurene,” *Nature Nanotechnol.*, vol. 15, no. 7, pp. 585–591, Jun. 2020.

[21] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2007, p. 332.

[22] H. Reisinger, O. Blank, W. Heinrigs, W. Gustin, and C. Schlünder, “A comparison of very fast to very slow components in degradation and recovery due to NBTI and bulk hole trapping to existing physical models,” *IEEE Trans. Device Mater. Rel.*, vol. 7, no. 1, pp. 119–129, Mar. 2007.

[23] P. D. Ye, “Main determinants for III–V metal-oxide-semiconductor field-effect transistors,” *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 26, no. 4, pp. 697–704, Jun. 2008.

[24] J. Robertson, “Model of interface states at III–V oxide interfaces,” *Appl. Phys. Lett.*, vol. 94, no. 15, Apr. 2009, Art. no. 152104.

[25] K. Xiong, J. Robertson, M. C. Gibson, and S. J. Clark, “Defect energy levels in HfO_2 high-dielectric-constant gate oxide,” *Appl. Phys. Lett.*, vol. 87, no. 18, Oct. 2005, Art. no. 183505.

[26] J. Robertson, “Band offsets of wide-band-gap oxides and implications for future electronic devices,” *J. Vac. Sci. Technol. B, Microelectron.*, vol. 18, no. 3, pp. 1785–1791, May 2000.

[27] P. D. C. King, T. D. Veal, D. J. Payne, A. Bourlange, R. G. Egdell, and C. F. McConville, “Surface electron accumulation and the charge neutrality level in In_2O_3,” *Phys. Rev. Lett.*, vol. 101, Sep. 2008, Art. no. 116808.

Authorized licensed use limited to: Purdue University. Downloaded on October 13,2022 at 17:17:37 UTC from IEEE Xplore. Restrictions apply.